XAVIER INSTITUTE OF ENGINEERING

A SISTER INSTITUTION OF ST. XAVIER'S COLLEGE

Guest lecture on "Overview of VLSI Design"

DATE: 3/9/2021

Event Coordinator(s)

1. Prof. Tejal Deshpande

Student Coordinator(s)

1. Spencer Lobo

Time & Place:

4th September,2021

11:30am to 1pm

Platform: Online (Google Meet)

Department:

EXTC

No of participants:

58

Dr. Sudhakar Mande, Associate Professor, Don Bosco Institute of Technology, Vidyavihar delivered a Guest lecture on "Overview of VLSI Design" on Saturday 4th September, 2021 for Third Year students of the Department of Electronics & Telecommunication.

Because of COVID-19 pandemic situation the guest lecture was conducted on Google Meet online platform.

60 participants from T.E attended the session. Some of the important topics covered were Applications of VLSI Design in Emerging Technologies, Opportunities in VLSI Industry, Performance parameter of CMOS logic circuits, types of Power dissipation, Low power techniques for digital circuits etc

The participants found it very informative and well organized. They look forward for more sessions on Future in VLSI Design

Signing Authority
Name and Designation

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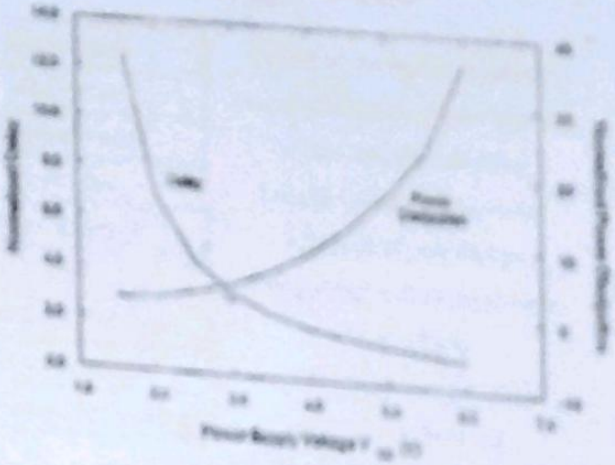
back from Participants:

session was great and interesting.
as helpful learnt something new
y helpful. Thank you.
e information provided by sir was really informative and helpful
ssion was great
elp us lot about vlsi design
teresting session
ecture was interesting but want to know more about this topic
ore such sessions
ood session
was an awesome session full of knowledge and interesting conceptual things. Hope for more such essions
Future of VLSI..
Keep organizing more lectures like this

Google form Link of the feedback taken -
https://docs.google.com/forms/d/1aubUYzKgD6Pe_Gk0ZzemtN2zsxi0Ng6PVHnj2Y2J_NU/edit

Low Power through Voltage Scaling



Low Power Techniques for Digital Circuits

- Using the lowest possible supply voltage
- Using smallest geometry devices
- Using parallel and pipelining mechanism to lower frequency of operation
- Power management by disconnecting power supply when the system is idle
- Circuit with multiple supply voltage and threshold voltage

Sudhakar Mande is presenting

System Levels for Energy Management

Application	Export computation to server
Algorithm	Variable resolution processing
Source Code	Improved code structure
Compiler	Energy-conscious compiler
Run-Time/O.S.	Just-in-time scheduling
Instruction Set	Energy-exposed architectures
Microarchitecture	Clock gating
Circuit Design	Low voltage-swing circuits
Fabrication Technology	SOI, Low-k dielectrics

Can usually combine savings at different levels

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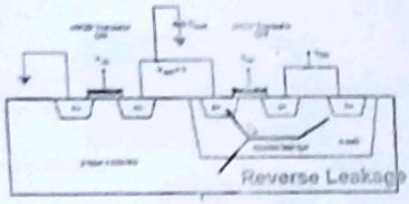
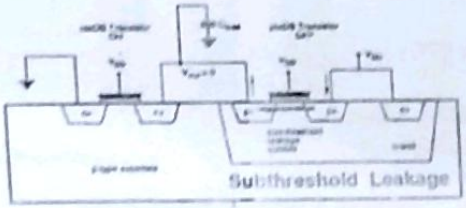
Sudhakar Mande is presenting

Leakage Power Dissipation





12:47 PM | eq2ceejj6j

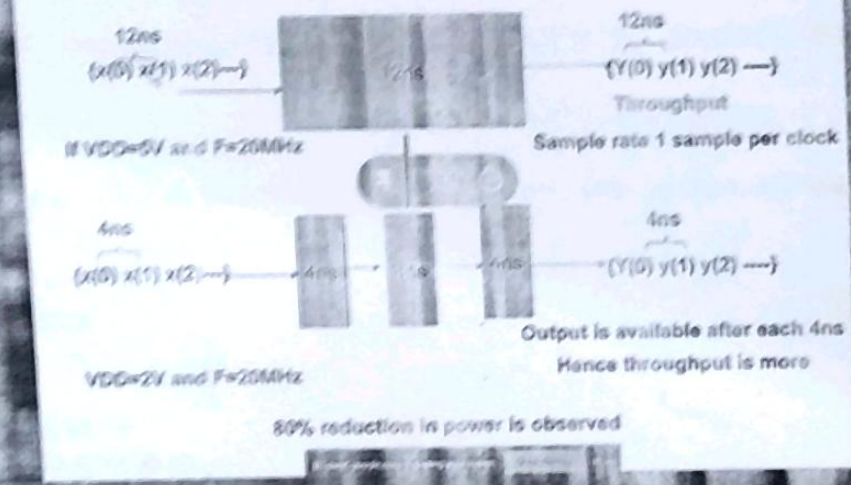
Sudhakar Mandla is presenting

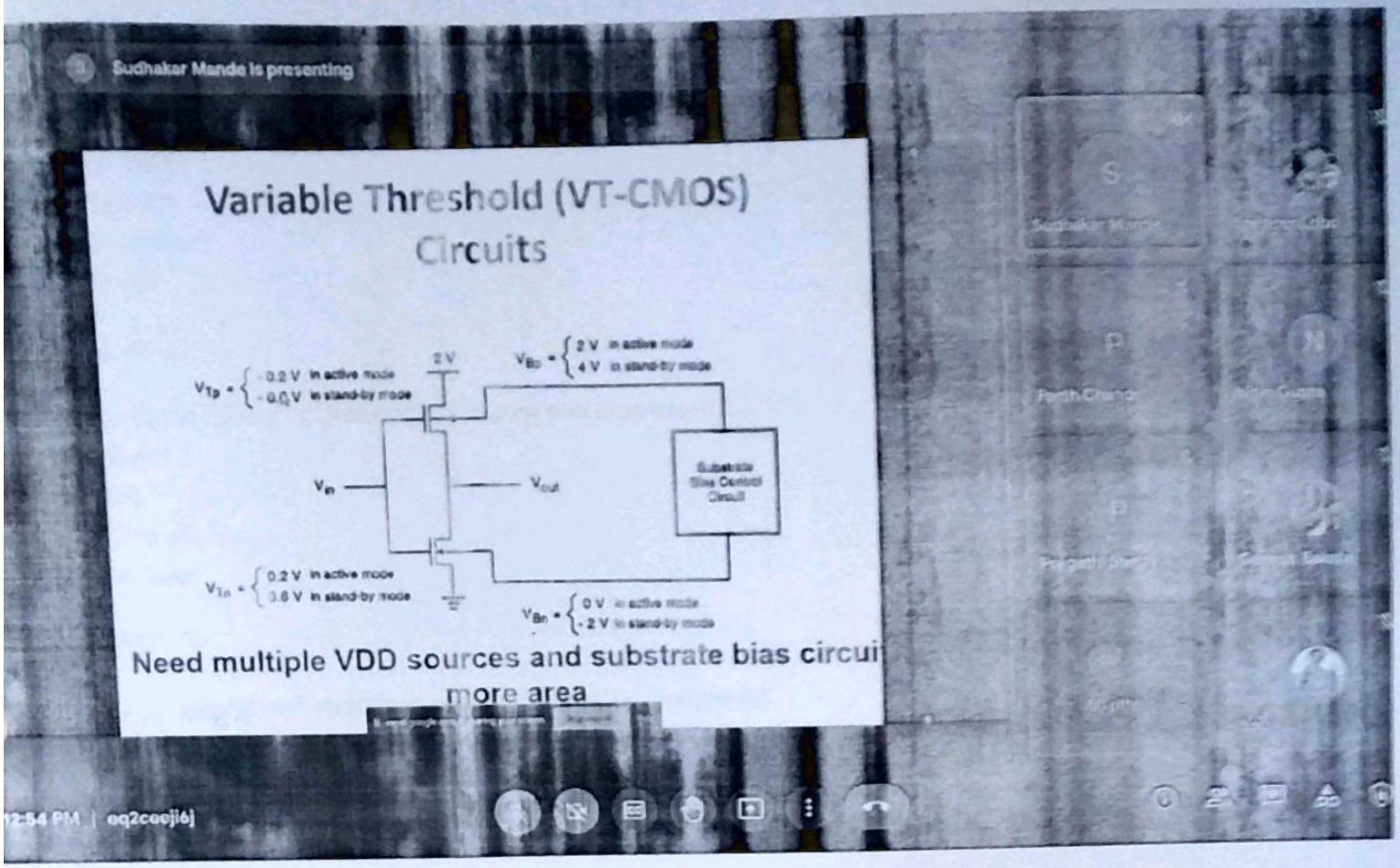
Opportunities in VLSI Industry

Gap Between Industry & Academia

Sudhakar Mandla is presenting

Concept of Pipelining





Attendance Link - https://docs.google.com/forms/d/1M8mmwwl24caO1PW_xzeWSLVQ3tE9YEEUi8Iln6SxzQQ/edit

MCQ Link - https://docs.google.com/forms/d/1i0ngIPsH3Qobwr1WJI6-PUE8UYerxX3tHofQQcW9IMDI/edit

MCQ Questions

1. National Policy on Electronics is released in --------year by Govt. of India.
   A. 2016
   B. 2017
   C. 2018
   D. 2019

   ANSWER: D

2. The purpose of National Policy on Electronics is to increase
   A. GDP
   B. TAX
   C. JOBS
   D. All of above

ANSWER: D

Which of the following is not Open source tool

A. Synopsis
B. Ngspice
C. Opentimer
D. Magic

ANSWER: A

4. Which of the following processor is design and developed by IIT B
   A. Shakti
   B. Ajit
   C. Celeron
   D. Skylane

   ANSWER: B

5. What is frequency of operation of first generation computer?
   A. 100Hz
   B. 100KHz
   C. 100MHz
   D. 1GHz

   ANSWER: C

6. What was the minimum feature size of MOSFET in the year 2015?
   A. 10um
   B. 6um
   C. 100nm
   D. 22nm

   ANSWER: D

7. Which of the following step is not used in IC fabrication?
   A. Etching
   B. Cleaning
   C. Diffusion
   D. Metallization

   ANSWER: B

8. During MOS fabrication process, which of the following Mask is used after active mask?
   A. Contact
   B. Gate
   C. Metallization
   D. None of above

ANSWER: B

How many mask are used in NMOS fabrication ?

A. 2
B. 3
C. 4
D. 5

ANSWER: C

10. Which of the following is not Performance metric in Digital VLSI?

A. Speed
B. Power
C. Gain
D. Area

ANSWER: C

11. In CMOS inverter tpLH depends on

A. Size of NMOS
B. Size of PMOS
C. Size of NMOS as well as PMOS
D. All of above

ANSWER: B

12. If two NMOS transistors each with trans conductance of Kn are connected in parallel, then what is trans conductan equivalent parallel combination ?

A. Kn
B. 2Kn
C. 0.5Kn
D. 1.5Kn

ANSWER: B

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